

AMD Turion™ 64 X2 Mobile Technology Dual-Core Processor Product Data Sheet



- **Compatible with Existing 32-Bit Code Base**
 - Including support for SSE, SSE2, SSE3*, MMX™, 3DNow!™ technology, and legacy x86 instructions
*SSE3 supported by Rev. E and later processors
 - Runs existing operating systems and drivers
 - Local APIC on the chip
- **AMD64 Technology**
 - AMD64 technology instruction set extensions
 - 64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses
 - Eight additional 64-bit integer registers (16 total)
 - Eight additional 128-bit SSE registers (16 total)
- **Dual-Core Architecture**
 - Discrete L1 and L2 cache structures for each core
- **Enhanced Virus Protection**
 - No Execute (NX) bit in page-translation tables specifies whether code can be executed from the page
- **HyperTransport™ Technology to I/O Devices**
 - One 16-bit link supporting speeds up to 800 MHz (1600 MT/s) or 3.2 Gbytes/s in each direction
- **64-Kbyte 2-Way Associative ECC-Protected L1 Data Cache**
 - Two 64-bit operations per cycle, 3-cycle latency
- **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**
 - With advanced branch prediction
- **16-Way Associative ECC-Protected L2 Cache**
 - Exclusive cache architecture—storage in addition to L1 caches
 - Up to 1 Mbyte per L2 cache
 - 1 Mbyte and 512-Kbyte options
- **Machine Check Architecture**
 - Includes hardware scrubbing of major ECC-protected arrays

Socket S1g1 Processor Specific Features

- **Refer to the *Socket S1g1 Processor Functional Data Sheet*, order# 31731, for functional and mechanical details of socket S1g1 processors. Refer to the *AMD NPT Family 0Fh Processor Electrical Data Sheet*, order# 31119, for electrical details of socket S1g1 processors.**
- **Packaging**
 - 638-pin lidless micro PGA package
 - 1.27-mm pin pitch
 - 26 x 26 pin grid array
 - 35 mm x 35 mm organic substrate
 - Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
- **Integrated Memory Controller**
 - Low-latency, high-bandwidth
 - 128-bit DDR2 SDRAM controller operating at up to 333 MHz
 - Supports up to two unbuffered SO-DIMMs
- **Electrical Interfaces**
 - HyperTransport™ technology: LVDS-like differential, unidirectional
 - DDR2 SDRAM: SSTL_1.8 per JEDEC specification
 - Clock, reset, and test signals also use DDR2 SDRAM-like electrical specifications.
- **Power Management**
 - Multiple low-power states including Deeper Sleep (C1E with AltVID)
 - System Management Mode (SMM)
 - ACPI compliant, including support for processor performance states
 - AMD PowerNow!™ technology is designed to dynamically switch between multiple low-power states based on application performance requirements.

Publication #	41407	Revision:	3.02
Issue Date:	September 2006		

Revision History

Date	Revision	Description
September 2006	3.02	Second public release. Added RoHS compliance statement for socket S1g1 processor-specific features.
August 2006	3.00	Initial public release.

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